PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Chang et al. (SANDP040) Conf. No. 2329

Serial No. 10/678,893 Group Art Unit: 2186

Filed: October 2, 2003 Examiner: Tsai

For: Hybrid Implementation for Error Correction Codes Within a Non-Volatile Memory System

APPELLANTS' REPLY BRIEF

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Appellants respectfully present their Reply Brief in response to the Examiner's Answer mailed September 20, 2007.

Appellants stand by their arguments as presented in the Amended Appellants' Brief filed July 4, 2007. This Reply Brief responds to certain points of argument presented in the Examiner's Answer, which were in response to Appellants' arguments in their main Brief.

Argument in response to the Examiner's Answer

Claim 4 and its dependent claim 3

Appellants maintain that the final rejection under §103 of claims 4 and 3 as unpatentable as unpatentable over the Bassett et al. reference[1] in view of the Yada et al. reference[2], and in the

[1] U.S. Patent No. 6,747,827 B1, issued June 8, 2004 to Bassett et al.

[2] U.S. Patent Application Publication US 2002/0032891 A1, published March 14, 2002, from an application filed August 27, 2001.

case of dependent claim 3, further in view of Applicants' admissions, is in error, for the reasons stated in their main Brief.

As mentioned above, Appellants will respond, in this Reply Brief, to certain points of argument raised in the Examiner's Answer, upon which the final rejection is maintained.

Patentable weight of the preamble of claim 4

Independent method claim 4 includes, in its preamble, the phrase "each of the plurality of blocks having an indicator indicative of whether the block is a reclaimed block". Claim 4 also includes a positively-recited method step that refers to the indicator introduced in the preamble: "responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm". However, in the Examiner's Answer, the Examiner asserts that the phrase "reclaimed block" appears only in the preamble of claim 4 and not elsewhere, and as such does not lend patentable weight.[3]

Appellants submit that the Examiner's interpretation of method claim 4 is in error as a matter of law.

The law of claim interpretation, regarding a term in a claim preamble, requires consideration of the claimed invention as a whole to determine the importance of the preamble term.[4] This consideration requires a determination of whether the preamble term gives meaning to other terms in the claim, in which case the preamble term is a claim limitation.[5] For example, whether a term in the preamble provides antecedent basis for language in the body of the claim is significant in concluding that the preamble is in fact a claim limitation.[6]

The *Bell Communications* case is particularly interesting in connection with claim 4 in this application. In that case, the claim at issue recited, in its preamble, a "method for

---

[3] Examiner's Answer, page 18, *citing* MPEP §2111.02[R-3], Section II.
[4] *Applied Materials Inc. v. Advanced Semiconductor Materials America, Inc.*, 98 F.3d 1563, 1573, 40 USPQ2d 1481, 1488 (Fed. Cir. 1996) ("Whether a preamble stating the purpose and context of the invention constitutes a limitation of the claimed process is determined on the facts of each case in light of the overall form of the claim, and the invention as described in the specification and illuminated in the prosecution history."); *Bell Communications Research, Inc. v. Vitalink Communications Corp.,* 55 F.3d 615, 620, 34 USPQ2d 1816, 1819-20 (Fed. Cir. 1995); MPEP §2111.02[R-3].
[5] *Porter v. Farmers Supply Service, Inc.*, 790 F.2d 882, 885, 229 USPQ 814, 816 (Fed. Cir. 1986).
[6] *Stranco Inc. v. Atlantes Chemical Systems Inc.,* 15 USPQ2d 1704, 1713 (S.D. Tex. 1990).

transmitting a packet over a system comprising a plurality of networks . . . said packet including a source address and destination address", while the body of the claim recited steps of "assigning, by said source device, one of said trees to broadcast *said* packet and associating with *said* packet an identifier indicative of said one of said trees".[7] A point of contention in that case was whether the preamble phrase "said packet including a source address and destination address" was to be given "definitional status" in interpreting the claim. The Federal Circuit found that this preamble phrase was a limitation of the claim because:

> These two steps of the claimed method, by referring to "*said* packet," expressly incorporate by reference the preamble phrase "said packet including a source address and a destination address." As a result, only a method for transmitting packet that have *both* source *and* destination addresses can literally infringe Claim 6.[8]

In the *Bell Communications* case, therefore, the limitations to the "packet" stated in the preamble were incorporated into the term "packet" used in the body of the claim.

Claim 4 on appeal in this application presents the identical situation. The preamble term at issue is "an indicator indicative of whether the block is a reclaimed block". The encoding step in the body of the claim is recited as being performed "responsive to *the indicator* associated with the first block meeting a criterion".[9] Following the Federal Circuit's decision in *Bell Communications*, therefore, the preamble limitation "indicative of whether the block is a reclaimed block" is expressly incorporated into the term "the indicator" in the body of the claim. It is therefore error to not give patentable weight to the limitation "indicative of whether the block is a reclaimed block".

To the extent that the final rejection of claim 4 and its dependent claim is based on the failure of the Examiner to give patentable weight to the term "reclaimed block", Appellants submit that the rejection is in error, as a matter of law, and should be reversed.

---

[7] *Bell Communications, supra,* USPQ at 1820 (emphasis in original).
[8] *Id.* (emphasis in original).
[9] Emphasis added.

Misinterpretation of the term "reclaimed block"

The Examiner maintains that the term "reclaimed block" is to be interpreted as "reused block", with "reused" apparently meaning "rewritten".[10] Based on this interpretation, the Examiner then combines the teachings of the Yada et al. reference regarding "frequently-rewritten parameter data" with the teachings of the Bassett et al. reference to reach the claims. Appellants submit that this interpretation is in error.

The claims of a patent or patent application are to be interpreted from the claim language itself, to consider its ordinary and customary meaning to a skilled artisan at the time of invention, in the context of the entire patent including the specification.[11] Reliance on the context of the invention is appropriate because patent claims do not stand alone, but are part of a fully integrated written instrument.[12]

Accordingly, to determine the meaning of "reclaimed block" in claim 4 of this application, one must consider the context of the entire patent including the specification. As previously urged in their main Brief,[13] the specification describes "reclaimed blocks" at length. Specifically, "reclaimed blocks" are defined as "blocks which were previously considered to be unusable blocks" but were "reclaimed for use after a rigorous testing process", such rigorous testing described in the specification itself and in another patent application to which reference is made.[14] In contrast, the specification of this application nowhere refers to blocks that have been erased many times (necessarily having been rewritten between erasures) as "reclaimed"; rather, these blocks are referred to as blocks with "high erase counts"[15] with the definition of "reclaimed blocks" clearly distinct from such blocks with "high erase counts" in the context of the specification.[16] Accordingly, the proper use of the context of the invention, including the

---

[10] Examiner's Answer, pages 18 and 19.
[11] *Phillips v. AWH Corp.,* 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2004)*; CCS Fitness, Inc. v. Brunswick Corp.,* 288 F.3d 1359, 62 USPQ2d 1658 (Fed. Cir. 2002)*; Johnson Worldwide Associates, Inc. v. Zebco Corp.,* 175 F.3d 985, 50 USPQ2d 1607 (Fed. Cir. 1999).
[12] *Phillips v. AWH Corp., supra.*
[13] Amended Appellants' Brief, pages 10 and 11.
[14] Specification of S.N. 10/678,893, page 18, line 10 through page 19, line 11.
[15] *See* specification, *supra, e.g.* at page 16, line 16 through page 18, line 8.
[16] The definition of "reclaimed blocks" immediately follows the discussion of "blocks with relatively high erase counts", and thus serves to distinguish the two types of blocks from one another. Specification, *supra,* page 18, lines 5 through 23.

specification itself, to interpret the term "reclaimed blocks" necessarily leads to the conclusion that the term "reclaimed block" does not refer to, and does not include, a flash memory block that is "reused" in the sense that it is "rewritten".

Furthermore, the context of the Yada et al. reference does not lead one to conclude that "reclaimed block" means the same thing as a "reused block", specifically a "rewritten block". This is because an indicator indicating whether a block has been rewritten one or more times would be of no practical use in the Yada et al. reference, nor in any flash memory. Actual flash memory blocks are re-writable; this re-writability is an important property of non-volatile flash memory devices.[17] Indeed, the Yada et al. reference itself clearly contemplates a large number of rewriting operations to individual blocks, considering its statement that "storage areas of the flash memory are successively switched and controlled every number of rewritings corresponding to 100 times".[18] Obviously, therefore, the Yada et al. reference contemplates that the blocks of its flash memory will be rewritten many times. In which case, there can be little or no functional use, according to the Yada et al. reference, for an indicator that is indicative of whether the block is a rewritten block –indeed, in connection with any flash memory including that described by Yada et al., there is no functional difference between a block that has never been rewritten and one that has been rewritten once. As such, the status of a conventional flash memory block as having been rewritten at least once is of no importance whatsoever.

In contrast, the status of whether a block has been "reclaimed", having been previously considered unusable but now considered as usable after a rigorous testing process, has been found by Appellants to be of importance, as deserving of different (*e.g.,* heightened) error correction coding. Claim 4 is, of course, directed to a method of storing data considering an indicator of this status.

Accordingly, Appellants submit that the two terms "reclaimed block" and "reused block" have different meanings from one another, especially if one follows the direction of the Federal Circuit to properly consider the context of the invention to interpret claim terms. The approach of the Examiner in maintaining the final rejection by interpreting the term "reclaimed block" to

[17] Yada et al., *supra,* paragraphs [0002] and [0003].
[18] *Id.*

mean "reused block", and by using this misinterpretation to combine the Yada et al. teachings with those of the Bassett et al. reference to reject claims 4 and 3 is therefore in error.

In conclusion

Appellants submit that these additional comments support their contention that the final rejection of claim 4 and its dependent claim is in error and should be reversed.

Claim 6 and its dependent claims

Appellants maintain that the final rejection, under §103, of claim 6 and certain of its dependent claims as unpatentable over the Bassett et al. reference in view of the Yada et al. reference is in error and should be reversed, for the reasons stated in their main Brief. Appellants also maintain their arguments as presented in their main Brief regarding the final rejection of dependent claims 7 through 10 and 13, as unpatentable over the Bassett et al. reference in view of the Yada et al. reference, and further in view of other references of record.

In this Reply Brief, however, Appellants will respond to a point of argument raised in the Examiner's Answer in response to Appellants' main brief.

In their main Brief, Appellants urged that none of the asserted references, including the Yada et al. reference, teaches or suggests the encoding of data according to a first or a second error detection algorithm, of different error detection capability, according to any attribute of the destination block in an array formed on a semiconductor substrate, much less responsive to an indicator having a value indicative of a number of times the block has been erased, as required by claim 6. In response to this argument, the Examiner asserted, *inter alia,* that:

i. Because the Yada et al. reference teaches:

> The present inventors have paid attention to the difference between the individual memory cell characteristics and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that the selection of an ECC method matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is

> reduced, whereby the use efficiency of the storage area is set to the maximum.[19]

the Yada et al. reference considers the characteristics of individual memory cells in determining the number of ECC code bits to be applied; and

ii. Because the Yada et al. reference teaches the selection of an ECC method based on the frequency of reuse of a memory block, the storage of such frequently-rewritten parameter data in a "specified partial storage area" using a particular ECC method, effectively matches the characteristics of a storage area with the nature of the data. In this regard, the Examiner uses an analogy of storing jewelry in a jewelry box and garbage in a garbage can to illustrate that the concept of matching a storage method to the data is the same as matching it to a characteristic of the storage location.

Appellants disagree with each of these points, as will now be discussed.

Regarding the assertion that the paragraph [0012] citation of the Yada et al. reference teaches "paying attention" to differences in individual memory cell characteristics in selecting an ECC code or method, Appellants submit that the Yada et al. reference discloses no way in which this "paying attention" amounts to actually analyzing a current indicator for a physical area of the memory to determine which ECC method to use, much less by obtaining an indicator associated with the identified block indicating the number of times the block has been erased, and encoding the data according to a comparison of that indicator to a threshold value as claimed.

So how *do* the Yada et al. inventors "pay attention" to differences in individual memory cell characteristics to select an ECC method? They do so by:

> optimiz[ing] functions or performance of plural storage areas so as to be suited to accomplishment of an end for the plural storage areas. It is appropriate to preferentially restrain a reduction in the reliability of information storage even if the use efficiency of each memory cell is sacrificed, because the degree of degradation in characteristic of each memory cell becomes high in, for example,

[19] Examiner's Answer, pages 22 and 23, *citing* Yada et al., *supra,* paragraph [0012] (emphasis added by the Examiner).

> storage applications such as parameters in which the number of rewritings is large, and preferentially maximize the use efficiency of each memory cell because the progress of degradation in characteristic becomes slow in an area in which the number of rewritings may be low.[20]

In other words, the Yada et al. reference teaches that the "degradation in characteristic of each memory cell" that occurs for frequently-rewritten data can be confined to a "partial storage area" in which error correction is applied, while program data are stored in other storage areas of the memory, without error correction.[21] As previously urged by Appellants in their main Brief, the Yada et al. reference teaches looking to the type of data being written (Is it "frequently-rewritten parameter data"? Or is it "program data"?) to determine the location into which that data is to be written, and therefore whether to apply error correction coding to that data. The result of this decision will be the same for a brand-new flash memory into which data has never been written, as it will be for a heavily-used memory nearing the end of its useful life – because the decision is made based on the nature of the data, rather than the nature of the memory.

In contrast, according to claim 6 on appeal in this case, however, one must obtain an indicator associated with the identified block, the indicator having a value indicative of a number of times that block has been erased; encoding of the data using a first or a second error detection algorithm is then performed responsive to whether the indicator is less than a threshold value, followed by writing the data into the identified block. According to this method, therefore, the data at issue are written into the same identified block in either case, regardless of the result of the decision of whether the indicator is less than the threshold. The selection of the first or the second error detection algorithm is made, however, based on the current value of the indicator that is indicative of the number of times the block has been erased. This indicator value will, of course, change over time – the same data written to the same block will be encoded with the first algorithm early in the life of the memory, but encoded with the second algorithm later in the life of the memory.

These substantial differences between the method of claim 6 and the alleged teachings of the Yada et al. reference stem directly from the difference in concept between this invention and

---

[20] Yada et al., *supra,* paragraph [0016] (emphasis added).
[21] *See, e.g.,* Yada et al., *supra,* paragraph [0029].

the Yada et al. reference. The Yada et al. reference "pays attention" to differences in the memory cells over time by making assumptions about how frequently the data is rewritten (past, present, and future) based on the nature of that data ("frequently-rewritten parameter data"), and selects a storage location and error correction accordingly. In contrast, the method of claim 6 makes no such assumptions based on the data – rather, it obtains an indicator of the number of times the identified destination block has been erased, and based on the current value of that indicator relative to a threshold value, encodes the data accordingly, in either case writing the data to the same destination block, namely the block associated with the indicator. Accordingly, the approach taken by the Yada et al. reference differs substantially from that claimed, because the Yada et al. reference teaches selection of ECC coding based on the nature of the data being written, as argued by Appellants in their main Brief.

The analogy suggested by the Examiner in the Examiner's Answer thus falls apart when one properly considers the teachings of the reference relative to the requirements of the claim. As the Examiner asserts, the Yada et al. teachings are indeed analogous to deciding to place valuable jewelry in a "safety box" and deciding to place garbage into a garbage can because, according to the reference, it is the nature of the thing being deposited that determines the container. But this analogy does not fit the method of claim 6. If Appellants can offer a poor analogy in response, the method of claim 6 is more like determining the size and number of holes in a fishing net, before deciding how big of a fish to put into the net.[22] Appellants' invention thus looks to the current state of the "container" before deciding the processing required of the "contents" to be stored in that "container"; in contrast, Yada et al. look to the contents (jewelry or trash) themselves, and choose a container (jewelry box or garbage can) accordingly.

For these reasons, Appellants maintain that the Examiner's application of the teachings of the Yada et al. reference in the final rejection of claim 6 and its dependent claims is in error. Appellants therefore maintain and urge reversal of this final rejection.

[22] *I.e.,* making sure that the fish is not so small that it will swim through the net.

Claim 16 and its dependent claims

Claim 16 includes the steps of obtaining an indicator indicative of a number of times an identified block has been erased, determining whether the indicator is less than a threshold value, and decoding data from that block according to a first or a second error detection algorithm responsive to that determination.

Appellants maintain their arguments relative to the final rejection of claim 16 and its dependent claims, as presented in their main Brief. In addition, Appellants' argument in this Reply Brief that is directed to the final rejection of claim 6 also apply to the points of argument raised in the Examiner's Answer regarding claim 16, and for those additional reasons submit that the Examiner's application of the teachings of the Yada et al. reference in the final rejection of claim 16 and its dependent claims is in error. Appellants therefore urge reversal of this final rejection of claim 16 and its dependent claims.

Claim 21 and its dependent claims

Claim 21 includes code devices for obtaining an indicator indicative of whether an identified block is a reclaimed block, code devices for encoding data using either a first or a second error detection algorithm responsive to whether that indicator meets a criterion, and code devices for writing the encoded data into that block.

Appellants maintain their arguments relative to the final rejection of claim 21 and its dependent claims, as presented in their main Brief. In addition, Appellants' argument in this Reply Brief that is directed to the final rejection of claim 4, relative to whether the term "reclaimed block" means the same as "reused block", also apply to the points of argument raised in the Examiner's Answer regarding claim 21.[23] For those additional reasons, as stated above, Appellants submit that the Examiner's application of the teachings of the Yada et al. reference in the final rejection of claim 21 and its dependent claims is in error. Appellants therefore urge reversal of this final rejection of claim 21 and its dependent claims.

[23] Appellants' argument presented above relative to claim 4, concerning whether the preamble ought to be afforded patentable weight, is not applicable to claim 21.

Claim 26 and its dependent claims

The memory system of claim 26 requires code devices for obtaining an indicator indicative of a number of times an identified block has been erased, code devices for determining whether the indicator is less than a threshold value, and code devices for encoding data from that block according to a first or a second error detection algorithm responsive to that determination, with code devices for writing the encoded data into the identified block.

Appellants maintain their arguments relative to the final rejection of claim 26 and its dependent claims, as presented in their main Brief. In addition, Appellants' argument in this Reply Brief that is directed to the final rejection of claim 6 also apply to the points of argument raised in the Examiner's Answer regarding claim 26, and for those additional reasons submit that the Examiner's application of the teachings of the Yada et al. reference in the final rejection of claim 26 and its dependent claims is in error. Appellants therefore urge reversal of this final rejection of claim 26 and its dependent claims.

Claim 33 and its dependent claims

The memory system of claim 33 requires code devices for obtaining an indicator indicative of a number of times an identified block has been erased, code devices for determining whether the indicator is less than a threshold value, and code devices for decoding data from that block according to a first or a second error detection algorithm responsive to that determination.

Appellants maintain their arguments relative to the final rejection of claim 33 and its dependent claims, as presented in their main Brief. In addition, Appellants' argument in this Reply Brief that is directed to the final rejection of claim 6 also apply to the points of argument raised in the Examiner's Answer regarding claim 33, and for those additional reasons submit that the Examiner's application of the teachings of the Yada et al. reference in the final rejection of claim 33 and its dependent claims is in error. Appellants therefore urge reversal of this final rejection of claim 33 and its dependent claims.

In conclusion

For the above reasons, Appellants respectfully maintain and supplement their position that the final rejection of the claims on appeal is in error, and should be reversed. Reversal of that final rejection is respectfully requested.

Respectfully submitted,

/Rodney M. Anderson/

Rodney M. Anderson
Registry No. 31,939
Attorney for Appellants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554